FAN5092

High Current System Voltage Buck Converter

Features

- Output from 1.1V to 5V
- Integrated high-current gate drivers
- Two interleaved synchronous phases per IC for maximum performance
- Up to 4 phase power system
- Built-in current sharing between phases and between ICs
- Frequency and phase synchronization between ICs
- Remote sense and Programmable Active Droop™
- High precision voltage reference
- High speed transient response
- Programmable frequency from 200KHz to 2MHz
- Adaptive delay gate switching
- Integrated Power Good, OV, UV, Enable/Soft Start functions
- Drives N-channel MOSFETs
- Operation optimized for 12V
- High efficiency mode at light load
- Overcurrent protection using MOSFET sensing
- 28 pin TSSOP package

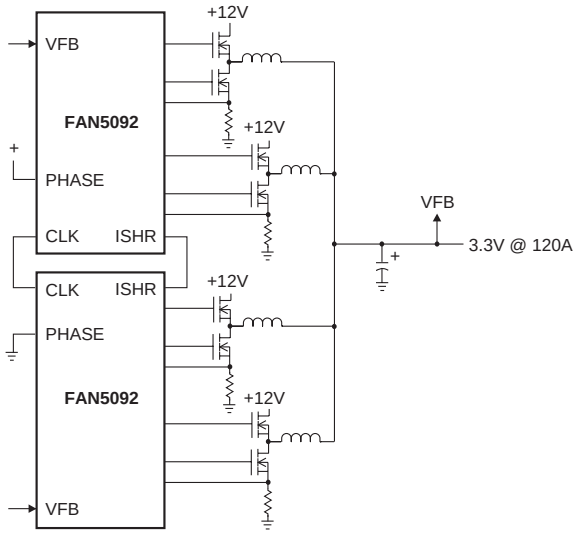
Applications

- Power supply for Logic
- Modular Power supply

Description

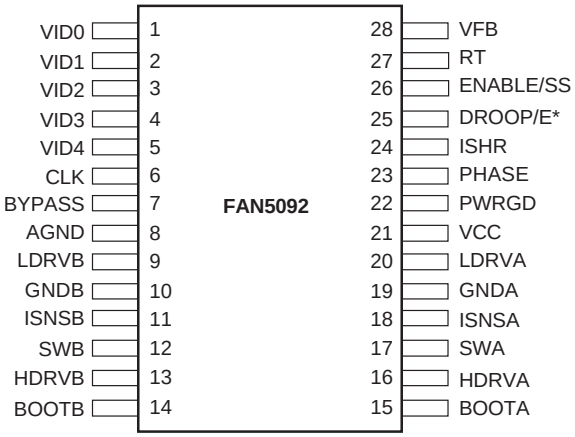
The FAN5092 is a synchronous multi-slice DC-DC controller IC which provides a highly accurate, programmable output voltage for all high-current applications. Two interleaved synchronous buck regulator phases with built-in current sharing operate 180° out of phase to provide the fast transient response needed to satisfy high current applications while minimizing external components. FAN5092s can be paralleled while maintaining both frequency and phase synchronization and ensuring current sharing in a high-power system. The FAN5092 features remote voltage sensing, Programmable Active Droop™ and advanced response for optimal converter transient response with minimum output capacitance. It has integrated high-current gate drivers with adaptive delay gate switching, eliminating the need for external drive devices. These make it possible to create power supplies running at a switching frequency as high as 4MHz, for ultra-high density. The output voltage can be set from 1.1V to 5V with an accuracy of 0.5%. The FAN5092 uses a high level of integration to deliver load currents in excess of 150A from a 12V source with minimal external circuitry. The FAN5092 also offers integrated functions including Power Good, Output Enable/Soft Start, under-voltage lockout, over-voltage protection, and current limiting with independent current sense on each slice. It is available in a 28-pin TSSOP package.

Block Diagram



Programmable Active Droop is a trademark of Fairchild Semiconductor.

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1-5	VID0-4	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1.
6	CLK	**Clock.** When PHASE is high, this pin puts out a clock signal synchronized 180° out of phase with the internal master clock. When PHASE is low, this pin is an input for a synchronizing clock signal.
7	BYPASS	**5V Rail.** Bypass this pin with a 0.1µF ceramic capacitor to AGND.
8	AGND	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
9	LDRVB	**Low Side FET Driver for B.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5”.
10	GNDB	**Ground B.** Ground-side current sense pin. Connect directly to low-side MOSFET source, or to sense resistor ground.
11	ISNSB	**Current Sense B.** Sensor side of current sense. Attach to low-side MOSFET drain, or to source side of sense resistor.
12	SWB	**High side driver source and low side driver drain switching node B.** Gate drive return for high side MOSFET, and negative input for low-side MOSFET current sense.
13	HDRVB	**High Side FET Driver B.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5”.
14	BOOTB	**Bootstrap B.** Input supply for high-side MOSFET.
15	BOOTA	**Bootstrap A.** Input supply for high-side MOSFET.
16	HDRVA	**High Side FET Driver A.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5”.
17	SWA	**High side driver source and low side driver drain switching node A.** Gate drive return for high side MOSFET, and negative input for low-side MOSFET current sense.
18	ISNSA	**Current Sense A.** Sensor side of current sense. Attach to low-side MOSFET drain, or to source side of sense resistor.

Pin Definitions (continued)

Pin Number	Pin Name	Pin Function Description
19	GNDA	**Ground A.** Ground-side current sense pin. Connect directly to low-side MOSFET source, or to sense resistor ground.
20	LDRVA	**Low Side FET Driver for A.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5”.
21	VCC	**VCC.** Internal IC supply. Connect to system 12V supply, and decouple with a 0.1µF ceramic capacitor.
22	PWRGD	**Power Good Flag.** An open collector output that will be logic LOW if the output voltage is not within +11/–12% of the nominal output voltage setpoint.
23	PHASE	**Phase Control.** Connecting this pin to bypass causes a synchronized clock signal to appear on CLK. Connecting this pin to ground allows the CLK pin to accept a clock signal for synchronization.
24	ISHR	**Current Share.** Connecting this pin to the ISHR pin of another FAN5092 enables current sharing.
25	DROOP/E*	**Droop Control/E*-mode Control.** A resistor from this pin to ground sets the amount of droop by controlling the gain of the current sense amplifier. Connecting this pin to bypass turns off Phase A.
26	ENABLE/SS	**Output Enable.** A logic LOW on this pin will disable the output. An internal current source allows for open collector control. This pin also doubles as soft start.
27	RT	**Frequency Set.** A resistor from this pin to ground sets the switching frequency. See Apps section.
28	VFB	**Voltage Feedback.** Connect to the desired regulation point at the output of the converter.

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
Supply Voltage VCC			15	V
Supply Voltages BOOTA, BOOTB			22	V
Voltage Identification Code Inputs, VID0-VID4			6	V
VFB, ENABLE/SS, PHASE, CLK			6	V
PWRGD			15	V
SW, ISNS	-3		15	V
PGNDA, PGNDB to AGND	-0.5		0.5	V
Gate Drive Current, peak pulse			3	A
Junction Temperature, T_J	-55		150	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature, 10 seconds		300		°C
Thermal Resistance Junction-to-case, Θ_{JC}		16		°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Driver Supply, Boot		16		17	V
V_{CC}		10.8	12	13.2	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C

Electrical Specifications

(V_{CC} = 12V, V_{OUT} = 1.500V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table I	•	1.100		1.850	V
Output Current				60		A
Internal Reference Voltage			1.4675	1.4750	1.4825	V
Initial Voltage Setpoint	I_{LOAD} = 5A		1.460	1.475	1.490	V
Output Temperature Drift	T_A = 0 to 70°C			-5		mV
Line Regulation	V_{IN} = 11.4V to 12.6V	•		+130		µV
Droop	I_{LOAD} = 0.8A to I_{max}		-90	-100	-110	mV
Programmable Droop Range	R_{DROOP} = TBD to TBD		-10		0	%V_{OUT}
Total Output Variation, Steady State[1]	I_{LOAD} = 0.8A to I_{max}	•	1.430		1.570	V
Total Output Variation, Transient[2]	I_{LOAD} = 0.8A to I_{max}	•	1.430		1.570	V
Response Time	ΔV_{OUT} = 10mV			100		nsec
Gate Drive On-Resistance				1.0		Ω
Upper Drive Low Voltage	V_{HDRV} – V_{SW} at I_{sink} = 10µA			0.2		V
Upper Drive High Voltage	V_{BOOT} – V_{HDRV} at I_{source} = 10µA			0.5		V
Lower Drive Low Voltage	I_{sink} = 10µA			0.2		V
Lower Drive High Voltage	V_{CC} – V_{LDRV} at I_{source} = 10µA			0.5		V
Output Driver Rise & Fall Time	See Figure 2			20		nsec
Current Mismatch	$R_{DS,on}$(A) = $R_{DS,on}$(B)			5		%
Output Overvoltage Detect		•	2.1		2.3	V
Efficiency	I_{LOAD} = I_{max}, I_{LOAD} = 2A, E*-mode enabled			85 70		%
Oscillator Frequency	RT = 41.2KΩ	•	450	600	750	KHz
Oscillator Range	RT = 125KΩ to 12.5KΩ		200		2000	KHz
Maximum Duty Cycle	RT = 125KΩ			90		%
Minimum LDRV on-time	RT=12.5KΩ			330		nsec
Input Low Current, VID pins	V_{VID} = 0.4V				50	µA
Soft Start Current				10		µA
Enable Threshold	ON OFF		 0.4		1.0	V
BYPASS Voltage			4.75	5	5.25	V

Electrical Specifications (continued)

(V_{CC} = 12V, V_{OUT} = 1.500V, and T_A = +25°C using circuit in Figure 1, unless otherwise noted.)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
BYPASS Capacitor			220	1000		nF
PWRGD Threshold	Logic LOW, minimum Logic LOW, maximum	• •	81 108	85 111	89 115	%V_{out}
PWRGD Hysteresis				20		mV
PWRGD Output Voltage	I_{sink} = 4mA				0.4	V
PWRGD Delay	High → Low			500		µsec
12V UVLO		•	8.5	9.5	10.5	V
UVLO Hysteresis				1.0		V
12V Supply Current	HDRV and LDRV open			20		mA
Over Temperature Shutdown				150		°C
Over Temperature Hysteresis				25		°C

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. Remote sensing should be used for optimal performance.

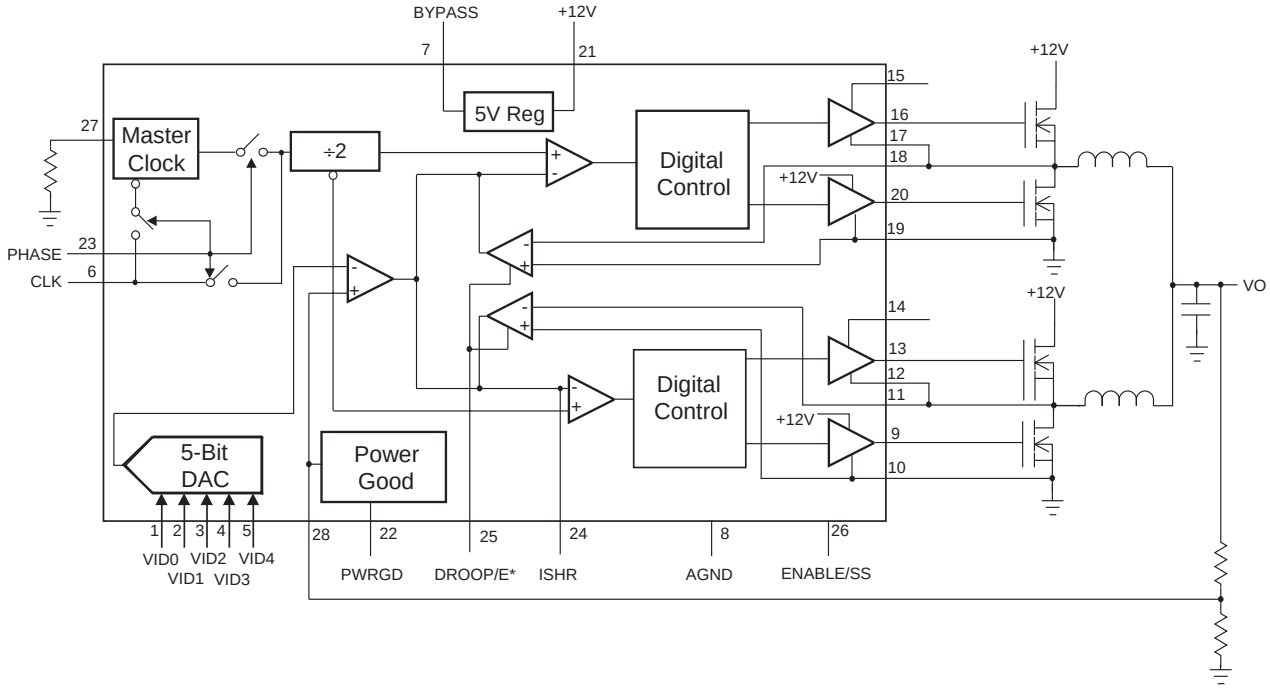
Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
1	1	1	1	1	OFF
1	1	1	1	0	1.100V
1	1	1	0	1	1.125V
1	1	1	0	0	1.150V
1	1	0	1	1	1.175V
1	1	0	1	0	1.200V
1	1	0	0	1	1.225V
1	1	0	0	0	1.250V
1	0	1	1	1	1.275V
1	0	1	1	0	1.300V
1	0	1	0	1	1.325V
1	0	1	0	0	1.350V
1	0	0	1	1	1.375V
1	0	0	1	0	1.400V
1	0	0	0	1	1.425V
1	0	0	0	0	1.450V
0	1	1	1	1	1.475V
0	1	1	1	0	1.500V
0	1	1	0	1	1.525V
0	1	1	0	0	1.550V
0	1	0	1	1	1.575V
0	1	0	1	0	1.600V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

Note:

1. 0 = VID pin is tied to GND.
   1 = VID pin is pulled up to 5V.

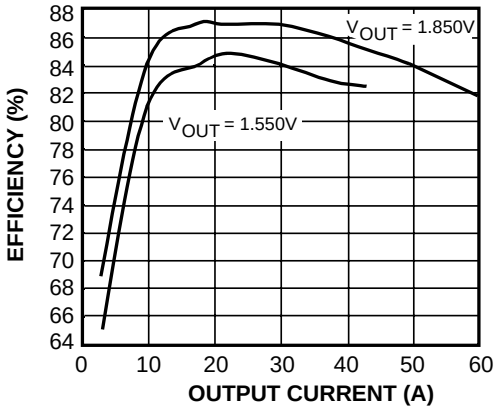
Internal Block Diagram



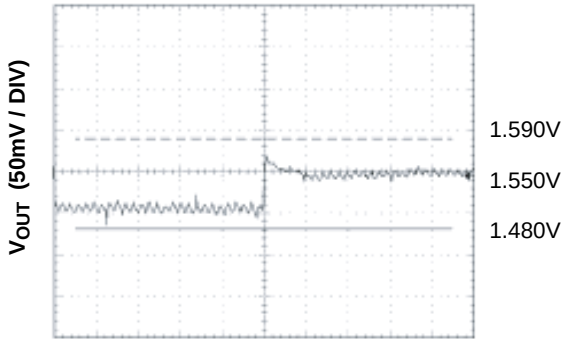
Typical Operating Characteristics

(V_{CC} = 12V, and T_A = +25°C using circuit in Figure 1 , unless otherwise noted.)

EFFICIENCY VS. OUTPUT CURRENT

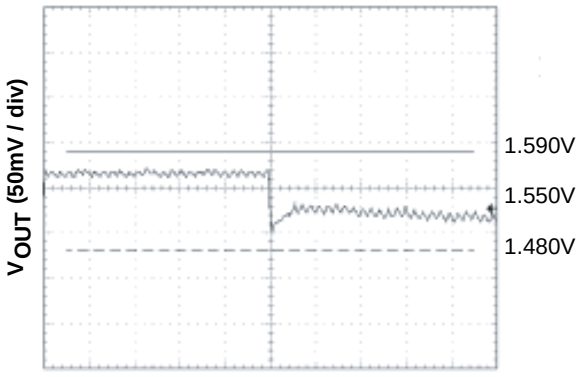


TRANSIENT RESPONSE, 50A to 0.5A



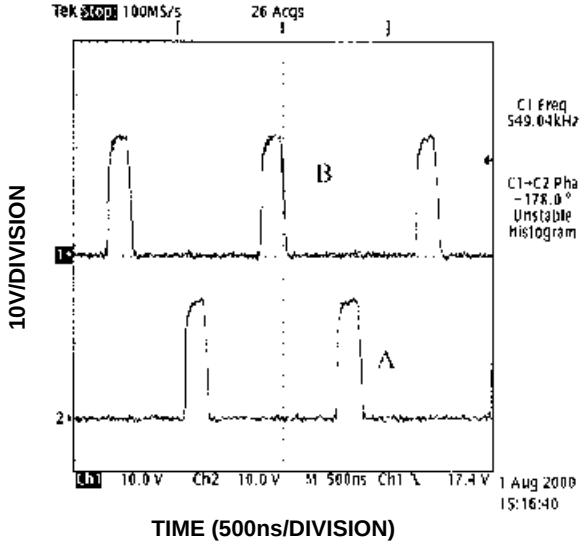
TIME (20µs/DIVISION)

TRANSIENT RESPONSE, 0.5A TO 50A



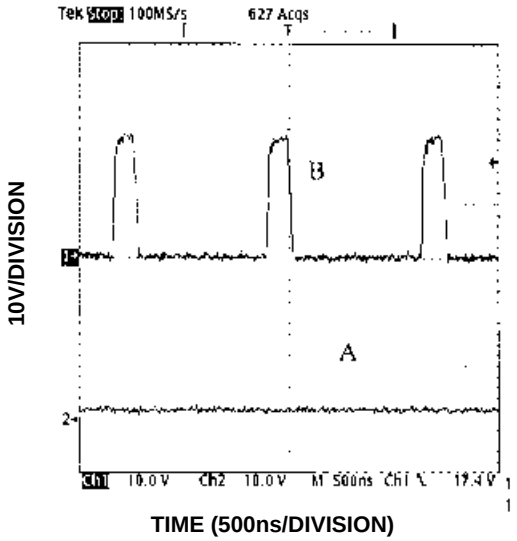
TIME (20µs/DIVISION)

HIGH-SIDE GATE DRIVES, NORMAL OPERATION



TIME (500ns/DIVISION)

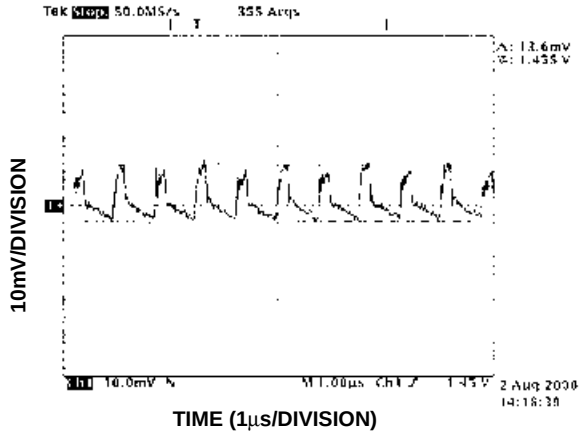
HIGH-SIDE GATE DRIVES, E*-MODE



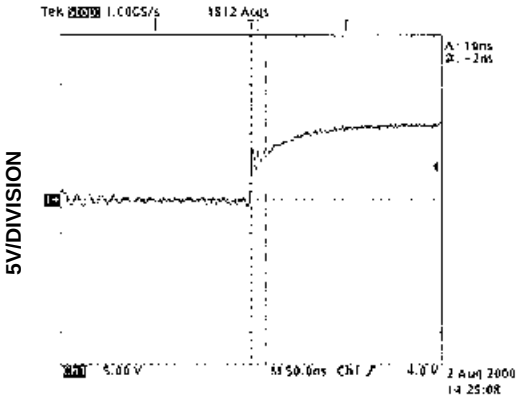
TIME (500ns/DIVISION)

Typical Operating Characteristics (Continued)

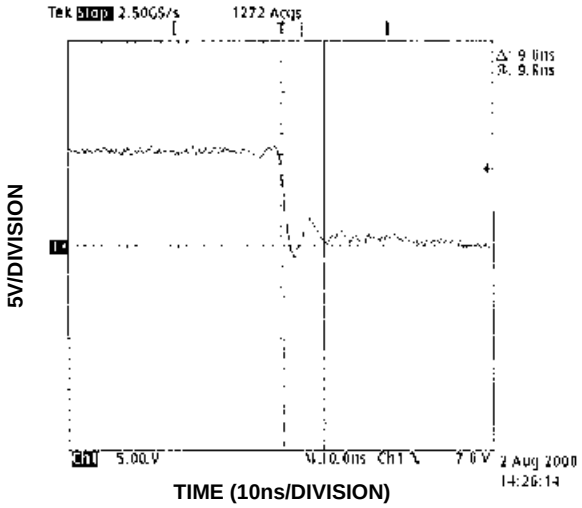
OUTPUT RIPPLE VOLTAGE



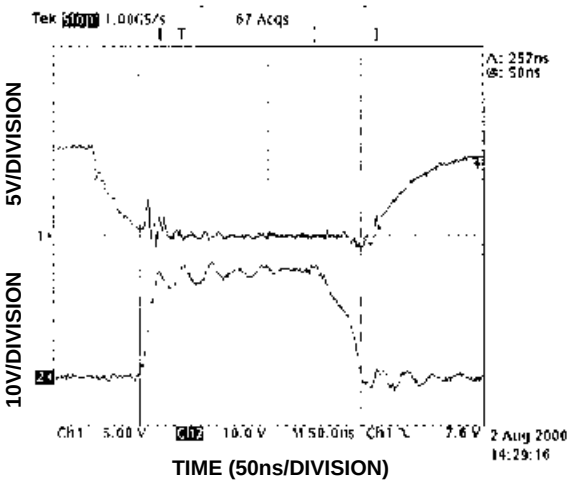
GATE DRIVE RISE TIME



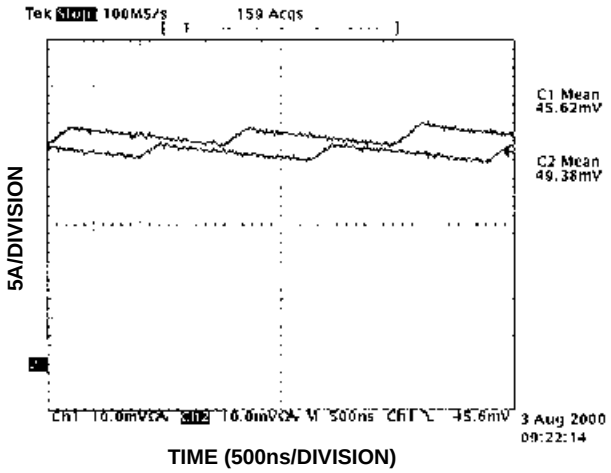
GATE DRIVE FALL TIME



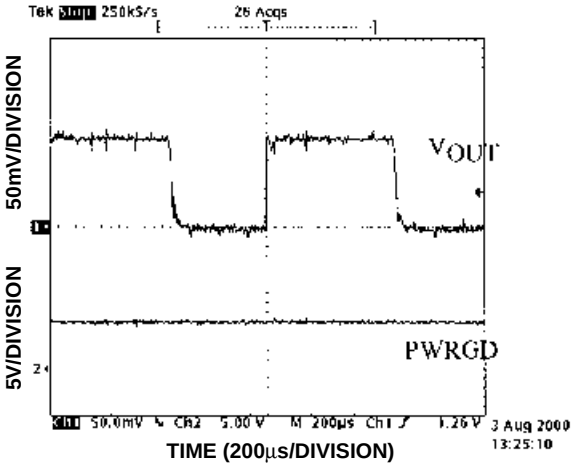
ADAPTIVE GATE DELAY



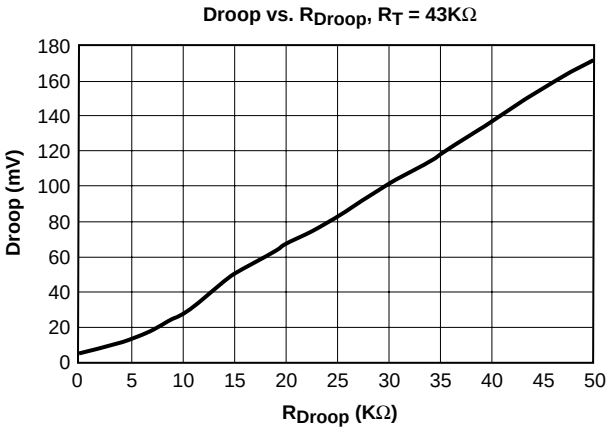
CURRENT SHARING BETWEEN INDUCTORS

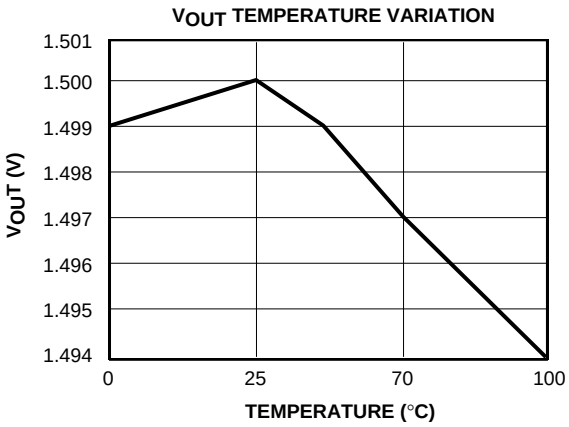


POWER GOOD DURING DYNAMIC VOLTAGE ADJUSTMENT



Typical Operating Characteristics (Continued)





Application Circuit

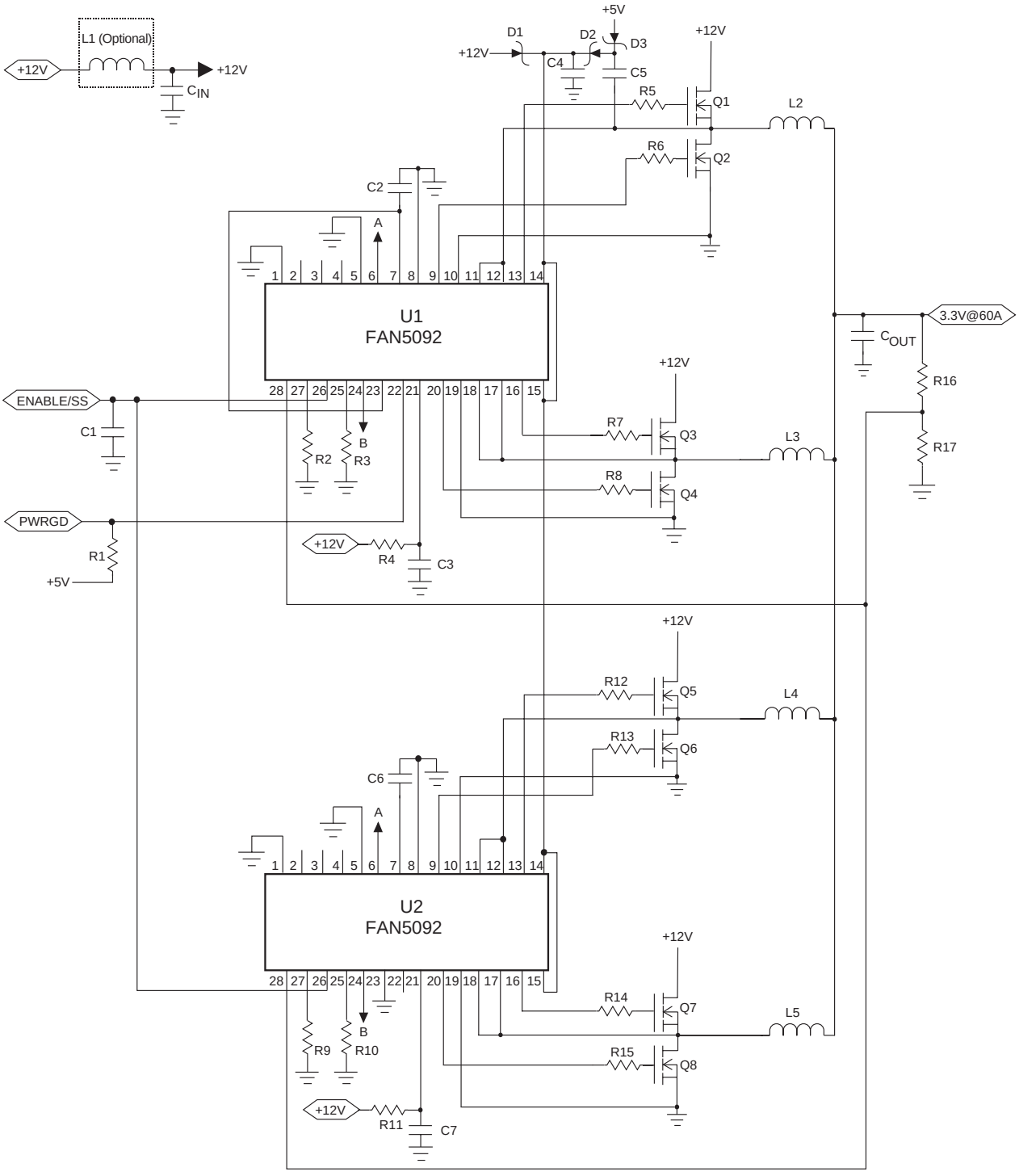


Figure 1. Four-Phase Application Circuit

Table 1. FAN5092 Application Bill of Materials for Figure 1

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1, C3-5, C7	Panasonic ECU-V1H104ZFX	5	100nF, 50V Capacitor	
C2, C6	Any	2	1µF Ceramic Capacitor	
C_{IN}	Rubycon 16ZL1000M	3	1000µF, 16V Electrolytic	I_{RMS} = 3.8A @ 65°C
C_{OUT}	Sanyo 4SP820M	12	820µF, 4V Oscon	ESR ≤ 12mΩ
D1-3	Fairchild MBR0520	3	0.5A, 20V Schottky Diode	
L1	Coiltronics DR127-1R5	Optional	1.5µH, 14A Inductor	DCR ~ 3mΩ. See Note 1.
L2-5	Coiltronics DR127-R47	4	470nH, 19A Inductor	DCR ~ 2mΩ
Q1, Q3, Q5, Q7	Fairchild FDB6035AL	4	N-Channel MOSFET	$R_{DS(ON)}$ = 17mΩ @ V_{GS} = 4.5V
Q2, Q4, Q6, Q8	Fairchild FDB6676S	4	N-Channel MOSFET with Schottky	$R_{DS(ON)}$ = 6.5mΩ @ V_{GS} = 10V
R1	Any	1	10KΩ	
R2, R9	Any	2	24.9KΩ	
R3, R10	Any	2	2KΩ	
R4, R11	Any	2	10Ω	
R5-8, R12-15	Any	8	4.7Ω	
R16	Any	1	243Ω	
R17	Any	1	200Ω	
U1-U2	Fairchild FAN5092M	1	DC/DC Controller	

Notes:

1. Inductor L1 is recommended to isolate the 12V input supply from noise generated by the MOSFET switching. L1 may be omitted if desired.
2. For a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

Test Parameters

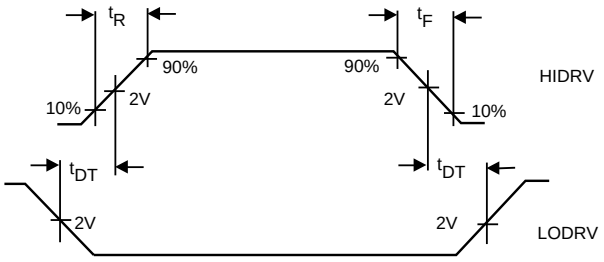


Figure 2. Output Drive Timing Diagram

Application Information

Operation

The FAN5092 Controller

The FAN5092 is a programmable synchronous multi-phase DC-DC controller IC. It can be run as a single controller, and a second FAN5092 can then be paralleled modularly for higher currents. When designed around the appropriate external components, the FAN5092 can be configured to deliver more than 120A of output current. The FAN5092 functions as a fixed frequency PWM step down regulator, with a high efficiency mode (E*) at light load.

Main Control Loop

Refer to the FAN5092 Block Diagram on page 7. The FAN5092 consists of two interleaved synchronous buck converters, implemented with summing-mode control. Each phase has its own current feedback, and there is a common voltage feedback.

The two buck converters controlled by the FAN5092 are interleaved, that is, they run 180° out of phase with each other. This minimizes the RMS input ripple current, minimizing the number of input capacitors required. It also doubles the effective switching frequency, improving transient response.

The FAN5092 implements “summing mode control”, which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads and external components.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts inputs from a current sensor and a voltage sensor, with the voltage sensor being common to both slices, and the current sensor separate for each. The voltage sensor amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to each of the two comparators. The current control path for each slice takes the difference between its PGND and SW pins when the low-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to the same input of its summing amplifier, adding its signal to the voltage amplifier’s with a certain gain. These two signals are thus summed together. This sum is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block. The oscillator ramps are 180° out of phase with each other, so that the two slices are on alternately.

The digital control block takes the analog comparator input to provide the appropriate pulses to the HDRV and LDRV output pins for each slice. These outputs control the external power MOSFETs.

Remote Voltage Sense

The FAN5092 has true remote voltage sense capability, eliminating errors due to trace resistance. To utilize remote sense, the VFB and AGND pins should be connected as a Kelvin trace pair to the point of regulation, such as the processor pins. The converter will maintain the voltage in regulation at that point. Care is required in layout of these grounds; see the layout guidelines in this datasheet.

High Current Output Drivers

The FAN5092 contains four high current output drivers that utilize MOSFETs in a push-pull configuration. The drivers for the high-side MOSFETs use the BOOT pin for input power and the SW pin for return. The drivers for the low-side MOSFETs use the VCC pin for input power and the PGND pin for return. Typically, the BOOT pin will use a charge pump as shown in Figure 1. Note that the BOOT and VCC pins are separated from the chip’s internal power and ground, BYPASS and AGND, for switching noise immunity.

Adaptive Delay Gate Drive

The FAN5092 embodies an advanced design that ensures minimum MOSFET transition times while eliminating shoot-through current. It senses the state of the MOSFETs and adjusts the gate drive adaptively to ensure that they are never on simultaneously. When the high-side MOSFET turns off, the voltage on its source begins to fall. When the voltage there reaches approximately 2.5V, the low-side MOSFETs gate drive is applied with approximately 50nsec delay. When the low-side MOSFET turns off, the voltage at the LDRV pin is sensed. When it drops below approximately 2V, the high-side MOSFET’s gate drive is applied.

Maximum Duty Cycle

In order to ensure that the current-sensing and charge-pumping work, the FAN5092 guarantees that the low-side MOSFET will be on a certain portion of each period. For low frequencies, this occurs as a maximum duty cycle of approximately 90%. Thus at 250KHz, with a period of 4µsec, the low-side will be on at least 4µsec • 10% = 400nsec. At higher frequencies, this time might fall so low as to be ineffective. The FAN5092 guarantees a minimum low-side on-time of approximately 330nsec, regardless of what duty cycle this corresponds to.

Current Sensing

The FAN5092 has two independent current sensors, one for each phase. Current sensing is accomplished by measuring the source-to-drain voltage of the low-side MOSFET during its on-time. Each phase has its own power ground pin, to permit the phases to be placed in different locations without affecting measurement accuracy. For best results, it is impor-

tant to connect the PGND and SW pins for each phase as a Kelvin trace pair directly to the source and drain, respectively, of the appropriate low-side MOSFET. Care is required in the layout of these grounds; see the layout guidelines in this datasheet.

Current Sharing

The two independent current sensors of the FAN5092 operate with their independent current control loops to guarantee that the two phases each deliver half of the total output current. The only mismatch between the two phases occurs if there is a mismatch between the $R_{DS,on}$ of the low-side MOSFETs.

In normal usage, two FAN5092s will be operated in parallel. By connecting the ISHR pins together, the two error amps of the two ICs will be forced to operate at exactly the same duty cycle, thus ensuring very close matching of the currents of all four phases.

Short Circuit Current Characteristics

The FAN5092 short circuit current characteristic includes a function that protects the DC-DC converter from damage in the event of a short circuit. The short circuit limit is given by the formula

$$I_{SC} = \frac{6V}{10 \bullet R_{DS,on}}$$

per phase.

Precision Current Sensing

The tolerances associated with the use of MOSFET current sensing can be circumvented by the use of a current sense resistor.

E*-mode

Further enhancement in efficiency can be obtained by putting the FAN5092 into E*-mode. When the Droop pin is pulled to the 5V BYPASS voltage, the “A” phase of the FAN5092 is completely turned off, reducing in half the amount of gate charge power being consumed. E*-mode can be implemented with the circuit shown in Figure 3:

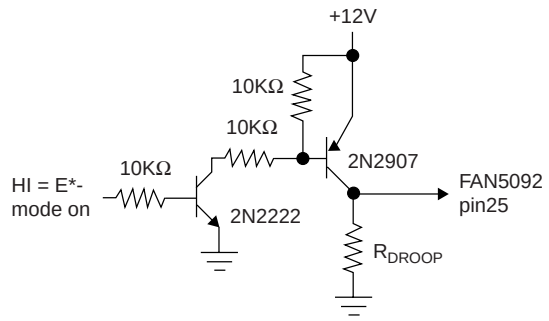


Figure 3. Implementing E*-mode Control

Note that the charge pump for the HIDRVs should be based on the “B” phase of the FAN5092, since the “A” phase is off in E*-mode.

Internal Voltage Reference

The reference included in the FAN5092 is a precision bandgap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC. The DAC monitors the 5 voltage identification pins, VID0-4, and scales the reference voltage from 1.100V to 1.850V in 25mV steps.

BYPASS Reference

The internal logic of the FAN5092 runs on 5V. To permit the IC to run with 12V only, it produces 5V internally with a linear regulator, whose output is present on the BYPASS pin. This pin should be bypassed with a 1µF capacitor for noise suppression. The BYPASS pin should not have any external load attached to it.

Dynamic Voltage Adjustment

The FAN5092 has interal pullups on its VID lines. External pullups should not be used. The FAN5092 can have its output voltage dynamically adjusted to accommodate low power modes. The designer must ensure that the transitions on the VID lines all occur simultaneously (within less than 500nsec) to avoid false codes generating undesired output voltages. The Power Good flag tracks the VID codes, but has a 500µsec delay transitioning from high to low; this is long enough to ensure that there will not be any glitches during dynamic voltage adjustment.

Power Good (PWRGD)

The FAN5092 Power Good function is designed in accordance with the Pentium IV DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage deviate more than +15%/-11% of its nominal setpoint. The output is guaranteed open-collector high when the power supply voltage is within +8%/-18% of its nominal setpoint. The Power Good flag provides no control functions to the FAN5092.

Output Enable/Soft Start (ENABLE/SS)

The FAN5092 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to soft-start the switching. A softstart capacitor may be approximately chosen by the formula:

$$C = \frac{t \bullet 10\mu A}{1 + V_{out}}$$

However, C must be ≥ 100nF.

Oscillator

The FAN5092 oscillator section runs at a frequency determined by a resistor from the RT pin to ground according to the formula

$$RT(\Omega) = \frac{50 \bullet 10^9}{f(Hz)}$$

The oscillator generates two square waves, 180° out of phase with each other. One is used internally, the other is sent to a second FAN5092 on the CLK pin.

The square wave generates two internal sawtooth ramps, each at one-half the square wave frequency, and running 180° out of phase with each other. These ramps cause the turn-on time of the two slices to be phased apart and the four phases to be 90° apart each. The oscillator frequency of the FAN5092 can be programmed from 400KHz to 4MHz with each phase running at 100KHz to 1MHz, respectively. Selection of a frequency will depend on various system performance criteria, with higher frequency resulting in smaller components but lower efficiency.

Programmable Active Droop™

The FAN5092 features Programmable Active Droop™: as the output current increases, the output voltage drops proportionately an amount that can be programmed with an external resistor. This feature is offered in order to allow maximum headroom for transient response of the converter. The current is sensed losslessly by measuring the voltage across the low-side MOSFET during its on time. Consult the section on current sensing for details. Note that this method makes the droop dependent on the temperature and initial tolerance of the MOSFET, and the droop must be calculated taking account of these tolerances. Given a maximum load current, the amount of droop can be programmed with a resistor to ground on the droop pin, according to the formula

$$R_{Droop}(\Omega) = \frac{2 \bullet n \bullet V_{Droop} \bullet RT}{I_{max} \bullet R_{DS,\,on}}$$

with V_{Droop} the desired droop voltage, RT the oscillator resistor, I_{max} the load current at which the droop is desired, and $R_{DS,\,on}$ the on-state resistance of one phase low-side MOSFET.

Typical response time of the FAN5092 to an output voltage change is 100nsec.

Important Note! The oscillator frequency must be selected before selecting the droop resistor, because the value of RT is used in the calculation of R_{Droop}.

Over-Voltage Protection

The FAN5092 constantly monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds 2.2V, an over-voltage condition is assumed and the FAN5092 latches on the external low-side MOSFET and latches off the high-side MOSFET. The DC-DC converter returns to normal operation only after V_{CC} has been recycled.

Thermal Design Considerations

Because of the very large gate capacitances that the FAN5092 may be driving, the IC may dissipate substantial power. It is important to provide a path for the IC's heat to be removed, to avoid overheating. In practice, this means that each of the pins should be connected to as large a trace as possible. Use of the heavier weights of copper on the PCB is also desirable. Since the MOSFETs also generate a lot of heat, efforts should be made to thermally isolate them from the IC.

Over Temperature Protection

If the FAN5092 die temperature exceeds approximately 150°C, the IC shuts itself off. It remains off until the temperature has dropped approximately 25°C, at which time it resumes normal operation.

Component Selection

MOSFET Selection

This application requires N-channel Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Drain-Source On-Resistance,
- $R_{DS,ON}$ < 10mΩ (lower is better);
- Power package with low Thermal Resistance;
- Drain-Source voltage rating > 15V;
- Low gate charge, especially for higher frequency operation.

For the low-side MOSFET, the on-resistance ($R_{DS,ON}$) is the primary parameter for selection. Because of the small duty cycle of the high-side, the on-resistance determines the power dissipation in the low-side MOSFET and therefore significantly affects the efficiency of the DC-DC converter. For high current applications, it may be necessary to use two MOSFETs in parallel for the low-side for each slice.

For the high-side MOSFET, the gate charge is as important as the on-resistance, especially with a 12V input and with higher switching frequencies. This is because the speed of the transition greatly affects the power dissipation. It may be a good trade-off to select a MOSFET with a somewhat higher $R_{DS,on}$, if by so doing a much smaller gate charge is available. For high current applications, it may be necessary to use two MOSFETs in parallel for the high-side for each slice.

At the FAN5092's highest operating frequencies, it may be necessary to limit the total gate charge of both the high-side and low-side MOSFETs together, to avert excess power dissipation in the IC.

For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Gate Resistors

Use of a gate resistor on every MOSFET is mandatory. The gate resistor prevents high-frequency oscillations caused by the trace inductance ringing with the MOSFET gate capacitance. The gate resistors should be located physically as close to the MOSFET gate as possible.

The gate resistor also limits the power dissipation inside the IC, which could otherwise be a limiting factor on the switching frequency. It may thus carry significant power, especially at higher frequencies. As an example, consider the gate resistors used for the low-side MOSFETs (Q2 and Q4) in Figure 1. The FDB7045L has a maximum gate charge of 70nC at 5V, and an input capacitance of 5.4nF. The total energy used in powering the gate during one cycle is the energy needed to get it up to 5V, plus the energy to get it up to 12V:

$$E = QV + \frac{1}{2}C \bullet \Delta V^2 = 70nC \bullet 5V + \frac{1}{2}5.4nF \bullet (12V - 5V)^2 = 482nJ$$

This power is dissipated every cycle, and is divided between the internal resistance of the FAN5092 gate driver and the gate resistor. Thus,

$$P_{Rgate} = \frac{E \bullet f \bullet R_{gate}}{(R_{gate} + R_{internal})} = 482nJ \bullet 300KHz \bullet \frac{4.7\Omega}{4.7\Omega + 1.0\Omega} = 19mW$$

and each gate resistor thus requires a 1/4W resistor to ensure worst case power dissipation.

The same calculation may be performed for the high-side MOSFETs, bearing in mind that their gate voltage swings only the charge pump voltage of 5V.

Inductor Selection

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. A smaller inductor produces greater ripple while producing better transient response. In any case, the minimum inductance is determined by the allowable ripple. The first order equation (close approximation) for minimum inductance for a two-slice converter is:

$$L_{min} = \frac{V_{in} - 2 \bullet V_{out}}{f} \bullet \frac{V_{out}}{V_{in}} \bullet \frac{ESR}{V_{ripple}}$$

where:
Vin = Input Power Supply
Vout = Output Voltage
f = DC/DC converter switching frequency
ESR = Equivalent series resistance of all output capacitors in parallel
Vripple = Maximum peak to peak output ripple voltage budget.

One other limitation on the minimum size of the inductor is caused by the current feedback loop stability criterion. The inductor must be greater than:

$$L \geq 3 \bullet 10^{-10} \bullet R_{DS,on} \bullet R_{Droop} \bullet (V_{in} - 2V_o)$$

where L is the inductance in Henries, $R_{DS,on}$ is the on-state resistance of one slice's low-side MOSFET, R_{Droop} is the value of the droop resistor in Ohms, V_{in} is either 5V or 12V, and V_o is the output voltage. For most applications, this formula will not present any limitation on the selection of the inductor value.

A typical value for the inductor is 1.3µH at an oscillator frequency of 1.2MHz (300KHz each slice) and 220nH at an oscillator frequency of 4MHz (1MHz each slice). For other frequencies, use the interpolating formula

$$L(nH) \approx \frac{1.86 \times 10^6}{f(KHz)} - 240$$

Schottky Diode Selection

The application circuit of Figure 1 shows a Schottky diode, D1 (D2 respectively), one in each slice. They are used as free-wheeling diodes to ensure that the body-diodes in the low-side MOSFETs do not conduct when the upper MOSFET is turning off and the lower MOSFETs are turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is extremely short, being minimized by the adaptive gate delay, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode. Power capability is not a criterion for this device, as its dissipation is very small.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance. For most converters, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low

ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

For higher frequency applications, particularly those running the FAN5092 oscillator at >1MHz, Oscon or ceramic capacitors may be considered. They have much smaller ESR than comparable electrolytics, but also much smaller capacitance.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; 0.1µF and 0.01µF are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system main supply and the converter input as shown in Figure 4. This inductor serves to isolate the main supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 1.3µH is recommended.

It is necessary to have some low ESR capacitors at the input to the converter. These capacitors deliver current when the high side MOSFET switches on. Because of the interleaving, the number of such capacitors required is greatly reduced from that required for a single-slice buck converter. Figure 5 shows 3 x 1000µF, but the exact number required will vary with the output voltage and current, according to the formula

$$I_{rms} = \frac{I_{out}}{4}\sqrt{4DC - 16DC^2}$$

for the four slice FAN5092, where DC is the duty cycle, DC = Vout / Vin. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-16.

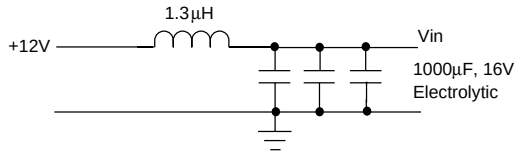


Figure 4. Input Filter

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 59.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the FAN5092 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the FAN5092 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the FAN5092. That is, traces that connect to pins 9-20 (LDRV, HDRV, GND and BOOT) should be kept far away from the traces that connect to pins 1 through 8, and pins 21-28.
- Place the 0.1µF decoupling capacitors as close to the FAN5092 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each power and ground pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky of a given slice as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the FAN5092 along with the PCAD layout Gerber file and silk screen can be obtained through your local Fairchild representative.

FAN5092 Evaluation Board

Fairchild provides an evaluation board to verify the system level performance of the FAN5092. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please contact your local Fairchild representative for an evaluation board.

Additional Information

For additional information contact your local Fairchild representative.

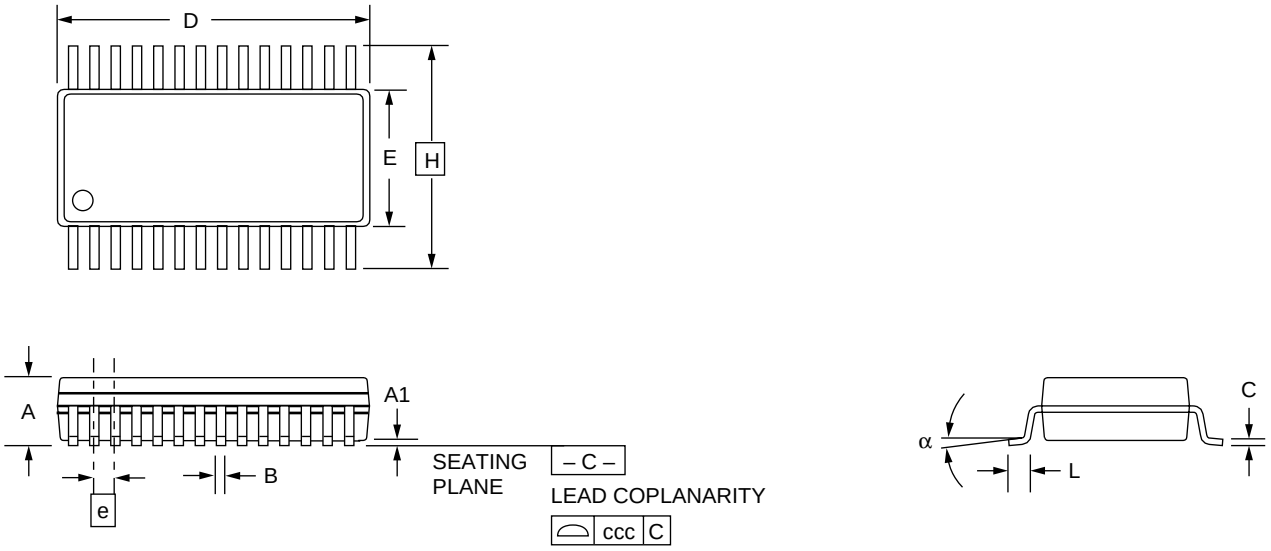
Mechanical Dimension

28 Lead TSSOP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.047	—	1.20	
A1	.002	.006	0.05	0.15	
B	.007	.012	0.19	0.30	
C	.008	.013	0.09	0.20	
D	.378	.386	9.60	9.80	2
E	.172	.180	4.30	4.50	2
e	.026 BSC		0.65 BSC		
H	.252 BSC		6.40 BSC		
L	.018	.030	0.45	0.75	3
N	28		28		5
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Package
FAN5092MTC	28 pin TSSOP
FAN5092MTCX	Tape & Reel